REMARKS

Figure 4 was inadvertently included with the original application. The October 1, 2001, Preliminary Amendment amended the specification to include references to Figure 4. Figure 4 has been cancelled, and the specification has been amendment to reflect the cancellation, and to correct a typographical error.

Further in reply to the Final Office Action of February 2, 2004, Applicant submits the following remarks. Each remark of the applicant below is preceded by a quotation of the related comments of the Examiner, shown in bold small type.

3. Claims l-3, 7-9 and 13 are rejected under 35 U. S. C. 103(a) as being unpatentable over Nielsen et al (US Patent No. 6,104,417) in view of Smith et al (US Patent No. 6,513,099).

4. As per claims 1 and 13, Nielsen et al substantially disclosed the invention as claimed, including a memory controller hub comprising: an internal graphics subsystem adapted to perform graphics operations on data (Fig. 2B; Item No. 218).

Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and available to an external graphics controller hub to store graphics data. However, Smith et al disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and available to an external graphics controller hub to store graphics data (Fig. 3, Item No. 3 14; col. 3, lines 13-20; col. 4, lines 59-67). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the memory controller disclosed by Smith et al into the system of Nielsen et al because doing so would provide a more flexible and expandable graphics system by allowing the memory controller to accommodate a plurality of I/O devices such as PCI Interface for providing PCI bus interface, routers, graphics interface and interface controller.

5. As per claim 7, Nielsen et al substantially disclosed the invention as claimed, including a CPU (Fig. 2, Item No. 206); a display device (col. 2, lines 48-50); a system memory adapted to store video data and non-video data (Fig. 2, Item No. 202); and a memory controller hub coupled to the CPU (Fig. 2, Item No. 204)and coupled to the system memory (Fig. 2, Item No. 202), the memory controller hub comprising: an internal graphics subsystem adapted to perform graphics operations on data (Fig. 2B; Item No. 218).

Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and available to an external graphics controller hub to store graphics data. However, Smith et al disclosed a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data and available to an external graphics controller hub to store graphics data (Fig. 3, Item No. 3 14; col. 3, lines 13-20; col. 4, lines 59-67). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized the memory controller disclosed by Smith et al into the system of Nielsen et al because doing so would provide a more flexible and expandable graphics system by allowing the memory controller to accommodate a plurality of I/O devices such as PCI Interface for providing PCI bus interface, routers, graphics interface and interface controller.

Applicant disagrees.

As the applicant stated in his Reply to the Office Action of June 11, 2003, the same cache is used for storing physical memory addresses available for use by an internal graphics subsystem and for storing physical memory addresses available for use by an external graphics controller.

As explained in the specification, the cache may be used, for example, to store Graphics Address Remapping Table (GART) entries (used by the external graphics controller in AGP mode) or Graphics Translation Table (GTT) entries (used by the internal graphics subsystem in Gfx mode). GART and GTT entries are used for translating virtual memory addresses into physical memory addresses. The specification explains an advantage of having a single cache that can store both GART and GTT entries: "Since the number of GART entries or GTT entries that may be stored in TLB 28 is limited by the physical die area size of the TLB, using the same TLB to store GART entries in AGP mode and to store GTT entries in Gfx mode effectively doubles the number of GART or GTT entries that may be stored in TLB compared to the number that could be stored if separate TLBs were used for GART and GTT entries." Specification at 9-10.

Nielsen discloses a graphics rendering and memory controller (item 218 in Fig. 2B). The controller supports a frame buffer address translation buffer (TLB) to translate frame buffer (x,y) addresses into physical memory addresses. Col. 6:37-39. However, as the Examiner appears to recognize, Nielsen does not disclose a memory controller hub (MCH) having a cache adapted to store addresses of locations in physical memory available to an external graphics controller coupled to the memory controller hub for storing graphics data, nor does Nielsen disclose an MCH having a cache that is adapted both to store addresses of locations in physical memory available to an external graphics controller coupled to the memory controller hub for storing graphics data and to store addresses of locations in physical memory available to an internal graphics controller for storing graphics data.

Smith does not remedy the failures of Nielsen. Smith discloses a cache for AGP based computer systems. Abstract. However, the cache in Smith is adapted for locally storing graphics data, which can then be fetched from the cache rather than from physical memory. See col. 2:9-18; col. 3:13-56. Thus, Smith's cache is adapted for storing graphics data themselves, is not adapted for storing addresses in physical memory that are available to a graphics controller for storing data, and bears little relation to the present invention. A cache for storing the addresses of physical memory locations available for the storage of graphics data is different from a cache for storing graphics data themselves.

Therefore, neither Nielsen nor Smith, nor the combination of the two discloses or suggests a memory controller hub having an internal graphics subsystem adapted to perform graphics operations on data and a cache adapted to store addresses of locations in physical memory available to the internal graphics subsystem for storing graphics data and adapted to store addresses of locations in physical memory available to an external graphics controller coupled to the memory controller hub for storing graphics data.

For at least the above reasons, applicant requests withdrawal of the rejection and allowance of the claims.

6. As per claims 2-3 and 8-9, Nielsen et al disclosed a dedicated bus interface coupling to the graphics controller to the memory controller hub (col. 4, lines 19-21).

Claims 2-3 depend from independent claim 1, and claims 8-9 depend from independent claim 7, and therefore claims 2-3 and 8-9 are allowable for at least the reasons explained above.

7. Claims 4-6, 10-12 and 14-16 are rejected under 35 U. S. C. 103(a) as being unpatentable over Nielsen al in view of Dye et al as applied to claims 1-3, 7-9 and 13 above, and further in view of Hussain et al (US Patent No. 6,667,745).

8. As per claims 4-6, 10-12 and 14-16, Nielsen et al did not disclosed a cache adapted to store addresses of locations in physical memory. However, Smith et al disclosed a cache adapted to store addresses of locations in physical memory (Fig. 3, Item No. 3 14; col. 3, lines 13-20; col. 4, lines 59-67).

The combination did not explicitly disclose that the memory controller is configured to provide a block of linear, virtual memory address for use by graphics subsystem or graphics controller. However, Hussain disclosed a graphics controller which utilizes tile frame buffer linear mapping system to perform mapping functions that facilitate mapping of linear virtual addresses to a physical memory address (col. 9, lines 25-38). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would not only allow the graphics system to communicate information to and from a memory in an efficient manner, including translation or conversion between different virtual address configurations and physical memory address, thereby enhance the processing speed of the graphics system.

Applicant does not understand the Examiner's reference to "Dye et al." This is the only mention of "Dye et al" in the Office Action, and the relevance of "Dye et al" is not explained in the Action. U.S. Patent No. 6,208,273 issued to Dye, Alvarez, and Geiger was listed in an Information Disclosure Statement filed by the applicant on December 10, 2003, but it is not clear if this is the reference to which the Examiner refers. Applicant respectfully requests the Examiner to explain his reference to "Dye et al" and its relevance to the present Office Action. See MPEP § 707.07.

Claims 4-6 depend from independent claim 1, claims 10-12 depend from claim 7, and claims 14-16 depend from independent claim, and are allowable at least for at least the reasons explained above.

In any case, Hussain does not remedy the failures of Nielsen and Smith. Hussain discloses a graphics controller (403) that receives information in a linear virtual address configuration and sends the information to a physical memory. Col. 9:25-38. The graphics controller uses a translation buffer 240 to map graphics tiles and determine a base address associated with a particular graphics tile. Col. 7:21-29; col. 8:13-49. However, Hussain does not disclose whether the graphics controller is external to a memory controller hub containing the translation buffer or if the translation buffer is internally integrated with a graphics subsystem in a memory controller. In any event, Hussain does not disclose or suggest a memory controller hub having a cache that is adapted both to store addresses of locations in physical memory available to an external graphics controller coupled to the memory controller hub for storing graphics data and to store addresses of locations in physical memory available to an internal graphics controller for storing graphics data.

For at least these reasons, applicant requests withdrawal of the rejection and allowance of the claims.

No fees are believed to be due at this time. Please apply any other charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10559-165001.

Respectfully submitted,

Date: 4-15-04

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